AMENDMENTS TO THE CLAIMS

By this Response, Applicant is amending Claims 1, 5, 6, 8, 10, 21, 30, 31 and 39 and is cancelling Claims 2–4, 11–15, 22, 23, 33 and 46 without prejudice or disclaimer. Claims 7, 9, 16–20, 24–29, 32, 34–38, 40–45, and 47–49 remain as originally filed.

1. (Currently Amended) A cache memory comprising:

a data memory configured to hold cache lines comprising a plurality of bytes of cache data; ~~and~~

a plurality of comparators, wherein each comparator has a first input coupled to said data memory such that each comparator receives one of said plurality of bytes of cache data via its associated first input, and wherein each comparator has a second input coupled to a second data source, such that the cache line may be compared to a test data string received from the second data source; and

a decoder coupled to an output of each comparator, the decoder configured to identify a location in the cache line that contains cache data that matches the test data string when matches from at least two of the plurality of comparators are detected in a comparison operation.

2.–4. (Cancelled)

5. (Currently Amended) The cache memory of Claim 1, wherein the test data string received from the second data source comprises a plurality of bytes.

6. (Currently Amended) The cache memory of Claim 5, wherein the test data string received from the second data source is a doubleword.

7. (Original) The cache memory of Claim 1, wherein the number of comparators is equal to the number of bytes in the cache line.

8. (Currently Amended) The cache memory of Claim 1, wherein the entire cache line is compared to the test data string received from the second data source in one clock cycle.

9. (Original) The cache memory of Claim 1, wherein the data memory comprises a Level 1 cache.

10. (Currently Amended) A cache memory for comparing a data value with data in a cache memory, the cache memory comprising:

a cache data memory configured to hold at least one cache line comprising a plurality of bytes of data;

a data source configured to hold a data value, wherein the data value comprises fewer bytes than the cache line;

a plurality of comparators configured to compare the cache line to the data value, each comparator having a first input coupled to said cache data memory and configured to receive at least one of said plurality of bytes of data, a second input coupled to the data source and configured to receive at least a portion of the data value from the data source, and an output; and

a decoder coupled to the outputs of the plurality of comparators and configured to identify a portion of the cache line that matches at least a portion of the data value when matches from at least two comparators are detected during a comparison operation.

11.–15. (Cancelled)

16. (Original) The cache memory of Claim 10, wherein the data value comprises a word.

17. (Original) The cache memory of Claim 10, wherein the number of the plurality of comparators is equal to the number of bytes in the cache line.

18. (Original) The cache memory of Claim 10, wherein the cache line is compared to the data value in one clock cycle.

19. (Original) The cache memory of Claim 10, wherein the data source comprises a processor.

20. (Original) The cache memory of Claim 10, wherein the cache data memory comprises a Level 1 cache.

21. (Currently Amended) A method for comparing cache memory data in a digital processing system with a test data string, the method comprising:

receiving an instruction to perform a compare operation, said instruction comprising a starting address and a test data string for use in said compare operation;

routing the instruction to a data string manipulation circuit;

routing the starting address for use in the compare operation from the data string manipulation circuit to a cache memory;

aligning the test data string with an offset of the starting address;

comparing the test data string with cached data stored in a cache line of the cache memory, wherein said test data string comprises fewer bytes than the cache line; and

routing an address of at least a portion of the cached data stored in the cache line of the cache memory that matches ~~matching~~ the test data string to the data string manipulation circuit.

22.–23. (Cancelled)

24. (Original) The method of Claim 21, wherein the data string manipulation circuit comprises a bus interface unit.

25. (Original) The method of Claim 21, wherein the data string manipulation circuit comprises a memory controller.

26. (Original) The method of Claim 21, wherein said act of comparing is performed by a plurality of subtractors.

27. (Original) The method of Claim 21, wherein said act of comparing is performed by a plurality of comparators.

28. (Original) The method of Claim 27, wherein the number of comparators is equal to the number of bytes in the cache line.

29. (Original) The method of Claim 21, wherein said act of comparing is performed in one clock cycle.

30. (Currently Amended) The method of Claim 21, wherein said act of routing an address of the matching cached data comprises routing the lowest numbered address if there are a plurality of matches [[in]] to the cache line.

31. (Currently Amended) A method for comparing a string of data in a cache memory with a test data string, the method comprising:

receiving an instruction to perform a compare operation, said instruction comprising a starting address for use in said compare operation;

routing the instruction to a data string manipulation circuit;

routing the starting address for use in the compare operation from the data string manipulation circuit to a cache memory array;

aligning a test data string with data stored in the cache memory array;

comparing [[a]] the test data string with the data stored in the cache memory array; and

routing an address of cached data matching the test data string to the data string manipulation circuit.

32. (Original) The method of Claim 31, additionally comprising routing the test data string from the data string manipulation circuit to the cache memory array.

33. (Cancelled)

34. (Original) The method of Claim 31, wherein the data string manipulation circuit comprises a bus interface unit.

35. (Original) The method of Claim 31, wherein the data string manipulation circuit comprises a memory controller.

36. (Original) The method of Claim 31, wherein said act of comparing is performed with a plurality of comparators.

37. (Original) The method of Claim 31, wherein said act of routing an address of the matching cached data comprises routing the lowest numbered address if there are a plurality of matches in the cache memory array.

38. (Original) The method of Claim 31, wherein said act of routing an address of cached data matching the test data is performed by a decoder.

39. (Currently Amended) A cache memory comprising:

a data source means for storing a test data;

a cache memory means for storing at least one cache line comprising a plurality of bytes of data;

a means for comparing the test data with the plurality of bytes of data, the means for comparing coupled to the data source means and to the cache memory means; and

a means for decoding coupled to the means for comparing, wherein the means for decoding is capable of identifying multiple ones of the plurality of bytes of data ~~identifies a portion~~ of the cache line that [[matches]] match at least a portion of the test data.

40. (Original) The cache memory of Claim 39, wherein the means for comparing comprises a plurality of comparators.

41. (Original) The cache memory of Claim 39, wherein the means for comparing comprises a plurality of subtractors.

42. (Original) The cache memory of Claim 39, wherein the data source means comprises an external string execution unit.

43. (Original) The cache memory of Claim 42, wherein the string execution unit comprises a bus interface unit.

44. (Original) The cache memory of Claim 42, wherein the string execution unit comprises a memory controller.

45. (Original) The cache memory of Claim 42, wherein the means for decoding is configured to forward a cache line address of the matching data to the string execution unit.

46. (Cancelled)

47. (Original) The cache memory of Claim 39, wherein the test data comprises a word.

48. (Original) The cache memory of Claim 39, wherein the entire cache line is compared to the test data in one clock cycle.

49. (Original) The cache memory of Claim 39, wherein the cache memory means comprises a Level 1 cache.